An FPGA-specific Approach to Floating-Point Accumulation and Sum-of-Products

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Outline

Context of this work

Proposed accumulator

Improved sum-of-products

Conclusions

Context of this work

Summing a large number of floating-point terms fast and accurately

Crucial for:

• Scientific computations:

- dot-product, matrix-vector product, matrix-matrix product
- numerical integration

• Financial simulations:

Monte-Carlo simulations

Floating-Point(FP) numbers

Let x be a **normalized** binary FP number:

$$x = (-1)^S \times 1.f \times 2^e$$

where:

- S the sign of x
- f the **fraction** of x.
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- e gives the dynamic range
 - IEEE-754 FP double precision, e_{min} =-1022 and $e_{max} = 1023$
- number of bits of f gives the **precision** p
 - IEEE-754 FP double precision, p=52

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Graphical representation:



	Addend		
Summands (shifted significands) Accumulator		Summands (shifted significands)	
Infinitely accurate accu	mulator	Floating-point accumulator	

	x0 Addend	0 0 1 1 1 1 0	100000		
Summands (shifted significands) <u>Accumulator</u>		Summands (s	shifted significands) oint		
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x0 00 Addend	. 1 1 1 0 1 0 0 0 0 0 0
x0 <u>1010000</u>	
Summands (shifted significands) Accumulator 100100000	Summands (shifted significands) floating point 0 0 1 1 1 1 0 1 0 0 0 0 0 0
Infinitely accurate accumulator	Floating-point accumulator

x1 0 1 0 0 1 0 Addend	2 0 1 0 0 1 1 0 0
x0 <u>1010000</u>	
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Accuracy:

Exact Result	=	50.2017822265625
FP Acc	=	50.125
Fixed-Point Acc	=	50.20166015625

Closer look



Accumulator based on combinatorial floating-point adder

- very low frequency
- must pipeline for larger frequency

Closer look



Accumulator based on pipelined floating-point adder

- loop's critical path contains 2 shifters
- shifters are deeply pipelined
- produces k accumulation results
- these results have to be added somehow
 - adder tree
 - multiplexing mechanism on accumulation loop

Closer look



Accumulator based on proposed long accumulator

- no shifts on the loop's critical path
- returns the result of the accumulation in fixed point
- the alignment shifter pipeline depth does not concern the result

Accumulator Architecture



- the sum is kept as a large fixed-point number
- one alignment shift (size depends on MaxMSB_X and LSB_A)
- the loop's critical path contains a fixed-point addition
- fixed-point addition is fast on current FPGAs

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- 64-bit addition works at 220MHz on Xilinx Virtex4 FPGA due to fast-carry chains
- still not enough ?
- use partial carry-save representation
 - cut large carry-propagation into chunks of k bits
 - critical path = k-bit addition
 - small cost: [width_{accumulator}/k] registers

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An **application tailored** fixed-point accumulator for **floating-point inputs**

Ensuring that:

- 1. accumulator significand never needs to be shifted
- 2. it never overflows
- 3. provides a result as accurate as the application requires





MSB_A the weight of the MSB of the accumulator
 must to be larger than max. expected result
 MaxMSB_X the max. weight of the MSB of the summand
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 determines the final accumulation accuracy



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How to chose the parameters using the rough error analysis ?

- MSB_A know an actual maximum + 10 bits safety margin
 - consider the number of terms to sum

$MaxMSB_X$ • exploit input properties + safety margin

- worst case: $MaxMSB_X = MSB_A$
- LSB_A precision vs. performance
 - consider the desired final precision
 - sum *n* terms, at most log₂ *n* bits are invalid

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Post-normalization unit, or not



converts fixed-point accumulator format to floating-point

- pipelined unit may be shared by several accumulators
- less useful:
 - many applications do not need the running sum
 - better to do conversion in software, use FPGA to accelerate the computation

Performance results



Performance results



Relative error results



Accumulation of $FP(w_E = 7, w_F = 16)$ in unif. [0,1] • LongAcc ($MSB_A = 20$, $LSB_A = -11$)

Accurate Sum-of-Products

Ideea

Accumulate exact results of all multiplications

- 1. Use exact multipliers:
 - return all the bits of the exact product
 - contain no rounding logic
 - are cheaper to build
- 2. Feed the accumulator with exact multiplication results

Cost: Input shifter of accumulator is twice as large

Operator Performance



Operator Performance



Operator Accuracy



Conclusion

- floating-point on FPGA should use the flexibility of the FPGA, not reimplement operators available in microprocessors
- faster and arbitrarily more accurate than a naive floating-point approach
- cost: designer-provided bounds on the accumulated values
- reward: improved performance + provably accurate accumulation
- available under GPL at: http://www.ens-lyon.fr/LIP/Arenaire/Ware/FloPoCo/

Thank you for your attention !

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• measuring only absolute error is not enough

• the error_{absolute} = $|x - \tilde{x}|$

example 1

x = 18234129837128312.192387123987 $\tilde{x} = 18234129837128312.192387123986$ $error_bankers = 1e - 12$

• example 2

 $\tilde{x} = 0.192307123986$

• better measure **relative error** (percentage error)

• $error_{rel} = \frac{\tilde{x} - x}{x}$

- example 1: $error_{rel} = -5e 29$
- example 2: $error_{rel} = -5e 12$

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